CELB-81

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Notes are used to call attention to information that is significant to the understanding and operation of equipment.

This BALOGH manual is based on information available at the time of its publication. We have attempted to provide accurate and up-to-date information. This document does not purport to cover all details or variations in hardware or software; nor does it provide for every possible combination of products. Some features described herein may not be available on all like products. BALOGH assumes no obligation to notify holders of this document of any subsequent changes.

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MANUAL REVISION HISTORY

Revision Description	Latest Revision Date	Revision Number	Approval Date
Address Change	04/12/10	3	04/12/10

Table of Contents

Introduction

The CELB-81 Control Board allows a host programmable controller running ladder logic to easily interface with the BALOGH RFID system. The BALOGH RFID system consists of the CELB-81 connected to a BALOGH Transceiver and a 24 VDC power supply.

Advantages

- **The CELB-81 can be instructed to Read or Write up to 77 bytes of data in Block Format.** This feature allows required TAG data to be Read and buffered in the CELB-81 in just one operation. This eliminates the need for multiple re-programming and re-reading steps when a TAG has arrived in the Transmission Zone.

- **The CELB-81 can be instructed to Read or Write up to 38 bytes of data in Discontinuous Format.** This feature can add speed and flexibility to a system whose critical data may be spread throughout the TAG'S memory map. This can also occur in one operation.

- **The CELB-81 can be pre-programmed by the PLC to await the appearance of a TAG.** This feature will allow for the automatic execution of the pre-programmed operation. With this feature all requested data is immediately available.

- **Discrete output for TAG Present signal**
- **Discrete output for General Fault signal**
- **Discrete output for Low Battery signal**
- **Transceiver Fault indication**
- **TAG Fault indication**
- **Reading and Writing occur at the same speed**
- **The CELB-81 can access all BALOGH OMA series Read/Write TAGS**
- **Requires minimal I/O**

Power Requirements

Voltage	24V regulated DC
Tolerance	-20% to +15% of 24V supply
Ripple Rejection	10%
Protection	Against DC polarity reversal
Max current drain	150mA board only

Transceiver Wiring

The CELB-81 is compatible with ERO, ERA, and TLEB BALOGH Transceiver styles.

The Transceiver can be located up to 300 meters from the control board. This link should be made with a 4-wire shielded cable (foil, braided, or both).

About the Shield:

Transceiver Side - Shield should end inside of the wiring chamber and be left unconnected (floating), protected by cable insulation.

Board Side - Shield should be terminated at the board's DC ground (terminal 31). If the shield must run unprotected for over 10cm then do not use shield. In this case let the shield float on the board side and be covered by the cable insulation.

NOTE: See Assembly Manual for cable recommendations.

CELB-81 to Transceiver Terminal Connections

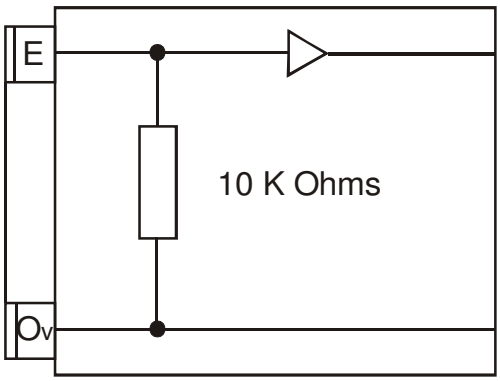
CELB-81 Terminal	Transceiver Symbol	Function
1	E	Transceiver Input
29	S	Transceiver Output
30	V	24 VDC
31	O	Ground

Inputs and Outputs

The following sections explain the Input/Output hardware responses of the control board in a Read/Write system.

Inputs

Inputs: 11 Sinking Inputs



Command Inputs

Terminal	Symbol	Function
17	WR	Program – Enables programming of the CELB-81
18	RD	Retrieve – Enables data retrieval after program execution
19	CK	Clock – Used to strobe commands, addresses, and data into the CELB-81

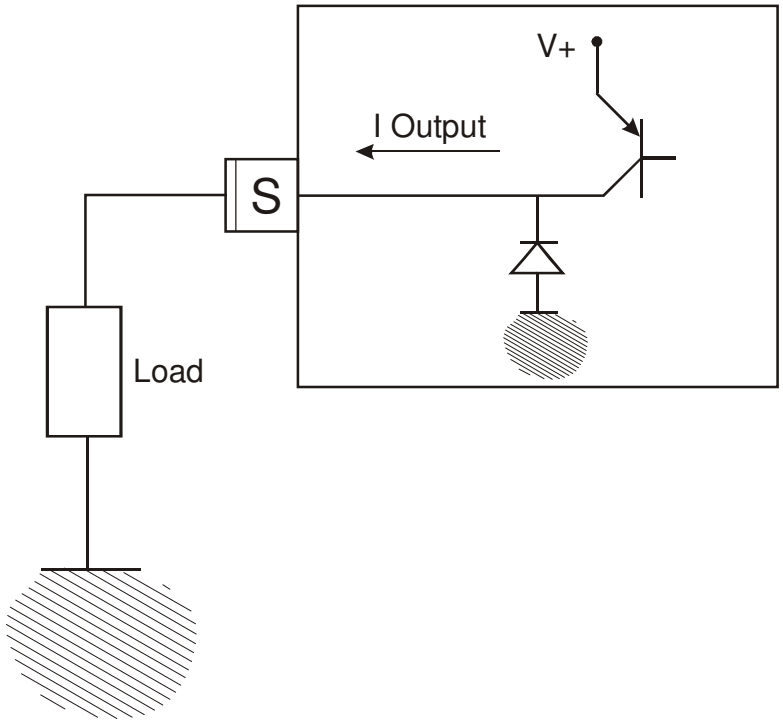
Data and Address Inputs

Terminal	Symbol	Function	
20	I-7	Address/Data	*MSB
21	I-6	Address/Data	
22	I-5	Address/Data	
23	I-4	Address/Data	
24	I-3	Address/Data	
25	I-2	Address/Data	
26	I-1	Address/Data	
27	I-0	Address/Data	**LSB

* Most Significant bit
** Least Significant bit

Outputs

Outputs: 14 Sourcing Outputs
Max. continuous current: 100mA
Logic 1 voltage: (V+)-1.5v
Leakage current in logic 0: 500uA
V+ = Positive DC supply voltage



Schematic Diagram

Status Outputs

Terminal	Symbol	Function
3	DEFB	Battery Fault – Low Battery
4	PRE	TAG Present – In Transceivers Transmission Zone
5	DF	Error Indicator
6	OC	Operation Complete
7	EC	In Process – Waiting for Command Execution
8	AK	Acknowledgement – Echo of CK Input

Data and Address Outputs

Terminal	Symbol	Function	
9	0-0	Address/Data	*MSB
10	0-1	Address/Data	
11	0-2	Address/Data	
12	0-3	Address/Data	
13	0-4	Address/Data	
14	0-5	Address/Data	
15	0-6	Address/Data	
16	0-7	Address/Data	**LSB

Parallel Protocol

Instructions are passed to the CELB-81 from the HOST via 11 Parallel Input lines. Responses from the CELB-81 Parallel Controller to the HOST are given via 14 Parallel Output lines.

The 11 Parallel Inputs consist of 8 Data Inputs and 3 Command Inputs (Program Input, Retrieve Data Input, and Clock Input).

The 14 Parallel Outputs consist of 8 Data Outputs and 6 Status Outputs (Operation in Process Output, Operation Complete Output, TAG Present Output, TAG Battery Low Output, General Fault Output, and Acknowledgement Output).

Operational Stages

Reading or Writing to a TAG takes place in three stages.

Stage 1: Board Programming

The CELB-81 receives through its Input Bus the following instructions from the HOST.

- Program code - 1 byte code, which instructs the CELB-81 to either, Read or Write, in Block or Discontinuous Format and targets the appropriate page of TAG memory.
- The number of bytes to Read or Write.
- The Address and/or Data associated with the programmed operation.

Stage 2: TAG Reading or Writing

This stage involves the actual Reading or Writing of a TAG. As the TAG enters into the Transceiver's Transmission Zone, dialogue takes place automatically. Successful completion of the operation is verified when the CELB-81 displays an Operation Complete signal.

Stage 3: Retrieving or Verifying Read or Written Data

After the CELB-81 indicates an Operation Complete signal the results of the operation can be retrieved or the HOST can decode a fault.

CELB-81 Program Code Table

Function	TAG Size	Target Memory	Program Code
Block Read	64 byte	Page 8 – Internal Ram	48H
Block Read	2K byte	Page 0 – 7	40H – 47H
Discontinuous Read	64 byte	Page 8 – Internal Ram	08H
Discontinuous Read	2K byte	Page 0 – 7	00H – 07H
Block Write	64 byte	Page 8 – Internal Ram	C8H
Block Write	2K byte	Page 0 – 7	C0H
Discontinuous Write	64 byte	Page 8 – Internal Ram	88H
Discontinuous Write	2K byte	Page 0 – 7	80H – 87H

The program code is the first byte entered into the CELB-81. It programs the board for a Read or Write in Block or Discontinuous format and also indicates the TAG page number.

EX: To Read page 3 of an OMA-831/2K TAG in Block Format the program code would equal 43H.

MSB	LSB
01000011	

Reading a TAG Block Format

Valid Program Codes: 40H TO 48H

Stage 1 CELB-81 Control Board programming

Action	Result
1. Set WR input to logic 1.	This puts the board in program mode. OC output will go to logic 0.
2. Set program code.	See TABLE 6.A. 48H 01001000
3. Set CK input to logic 1.	AK output will go to logic 1.Program code will be echoed to Output Bus.
4. Set number of bytes to block read on Input Bus.	
5. Set CK input to logic 0.	AK output will go to logic 0.Number of bytes will be echoed to the Output Bus.
6. Set starting TAG read address on Input Bus.	
7. Set CK input to logic 1.	AK output will go to logic 1. Starting address will be echoed to the Output Bus.
8. Set CK and WR inputs to logic 0.	AK output will go to logic 0. EC output will go to logic 1. Output Bus will clear to 0. Program is complete.

The Block Read command is now loaded into the CELB-81.

Stage 2 Reading the TAG

1.	TAG enters into the Transceivers Transmission Zone. PRE will go to logic 1.
2.	The CELB-81 executes the programmed instruction and performs an absolute Data check
3.	The EC output will go to logic 0.
4.	Operation Complete output will go to logic 1. This indicates the instruction has been successfully completed.

Stage 3 Retrieving the Data Read from the TAG

Action	Result
1. Set RD input to logic 1.	
2. Set CK input to logic 1.	AK output will go to logic 1. Output Bus will echo the program code for the instruction just executed
3. Set CK input to logic 0.	AK output will go to logic 0. Output Bus will echo the number Of bytes Read.
4. Set CK input to logic 1.	AK output will go to logic 1. Output Bus will echo the Data Read from the first TAG address.
5. Set CK input to logic 0.	AK output will go to logic 0. Output Bus will echo the Data Read from the second TAG address.
6. Repeat 4 and 5 until all Data read from the TAG has been retrieved.	
7. Set CK input to logic 0.	
8. Set RD input to logic 0.	Output Bus will clear to 0.

Reading a TAG Discontinuous Format

Valid Program Codes: 00H TO 08H

Stage 1 CELB-81 Control Board Programming

Action		Result
1.	Set WR input to logic 1.	This puts the board in program mode. OC output will go to logic 0.
2.	Set program code for discontinuous format.	
3.	Set CK input to logic 1.	AK output will go to logic 1. Program code will be echoed to Output Bus.
4.	Set number of bytes to be Read.	8H 00001000
5.	Set CK input to logic 0.	AK output will go to logic 0. Number of bytes will be echoed to the Output Bus.
6.	Set first TAG address to be Read.	
7.	Set CK input to logic 1.	AK output will go to logic 1. First address will echo to Output Bus.
8.	Set second TAG address to be Read.	
9.	Set CK input to logic 0.	AK output will go to logic 0. Second address will echo to Output Bus.
10.	Repeat steps 6 to 9 until all TAG addresses are loaded.	
11.	Set CK and WR inputs to logic 0 to end programming.	AK output will go to logic 0. EC output will go to logic 1. Output Bus will clear to 0.

The Discontinuous Read command is now loaded into the CELB-81. The presence of a TAG in the Transceiver's Transmission Zone field is not necessary.

Stage 2 Reading a TAG

1. TAG enters Transceiver zone. PRE will go to logic 1.
2. The CELB-81 executes the programmed instruction and performs an absolute Data check.
3. The EC output will go to logic 0.
4. Operation Complete output will go to logic 1. This indicates the instruction has been successfully completed.
5. When the TAG leaves the Transceivers Transmission Zone, PRE output will go to logic 0.

Stage 3 Retrieving Data Read from TAG

Action		Result
1.	Set RD input to logic 1.	
2.	Set CK input to logic 1.	AK output will go to logic 1. The Output Bus will echo the program code for the instruction just executed.
3.	Set CK input to logic 0.	AK output will go to logic 0. Output Bus will echo the number of bytes it read.
4.	Set CK input to logic 1.	AK output will go to logic 1. Output Bus will echo the Data Read from the first TAG address.
5.	Set CK input to logic 0	AK output will go to logic 0. Output Bus will echo the Data Read from the second TAG address.
6.	Repeat 4 and 5 until all Data Read from the TAG has been retrieved.	
7.	Set CK and RD inputs to logic 0.	Output Bus will clear to 0.

Writing to a TAG Block Format

Valid Program Codes: C0H TO C8H

Stage 1 CELB-81 Control Board Programming.

Action	Result
1. Set WR input to logic 1.	This puts the board in program mode. OC output will go to logic 0.
2. Set program code for Block Write format.	C8H 11001000
3. Set CK input to logic 1.	AK output will go to logic 1. Program code will be echoed to Output Bus.
4. Set number of bytes to be Block Written.	
5. Set CK input to logic 0.	AK output will go to logic 0. Number of bytes will be echoed to the Output Bus
6. Set starting TAG Write address.	
7. Set CK input to logic 1.	AK output will go to logic 1. Starting address will echo to the Output Bus.
8. Set first Data to Write.	
9. Set CK input to logic 0.	AK output will go to logic 0. First Data will echo to Output Bus.
10. Set second Data to Write.	
11. Set CK input to logic 1.	AK output will go to logic 1. Second Data will echo to Output Bus.
12. Repeat 8 to 11 until all Data to be Written is loaded.	
13. Set CK and WR inputs to logic 0.	AK output will go to logic 0. EC output will go to logic 1. Output Bus will clear to 0.

The Block Write command is now loaded into the CELB-81. The presence of a TAG in the Transceivers Transmission Zone is not necessary.

Stage 2 Writing to the TAG

1.	TAG enters Transceiver Transmission Zone. PRE will go to logic 1.
2.	The CELB-81 executes the programmed instruction and performs an absolute Data check.
3.	The EC output will go to logic 0.
4.	OC output will go to logic 1. This indicates the instruction has been successfully completed.
5.	When the TAG leaves the Transceiver Transmission Zone, PRE output will go to logic 0.

Stage 3 Verifying Command Execution.

Action	Result
1. Set RD input to logic 1.	
2. Set CK input to logic 1.	AK output will go to logic 1. The Output Bus will echo the program code for the instruction just executed.
3. Set CK input to logic 0.	AK output will go to logic 0. Output Bus will echo the number of bytes it wrote.
4. Set CK input to logic 1.	AK output will go to logic 1. Output Bus will echo the Data Written to the first TAG address.
5. Set CK input to logic 0.	AK output will go to logic 0. Output Bus will echo the Data Written to the second TAG address.
6. Repeat 4 and 5 until all Data Written to the TAG has been verified.	
7. Set CK input to logic 0.	
8. Set RD input to logic 0.	Output Bus will clear to 0.

Writing to a TAG Discontinuous Format

Valid Program Codes: 80H TO 88H

Stage 1 CELB-81 Control Board Programming

Action		Result
1.	Set WR input to logic 1.	This puts the board in program mode. OC output will go to logic 0.
2.	Set desired program code for discontinuous format.	88H 10001000
3.	Set CK input to logic 1	AK output will go to logic 1. Program code will be echoed to Output Bus.
4.	Set number of bytes to be Written.	
5.	Set CK input to logic 0.	AK output will go to logic 0. Number of bytes will echo to the Output Bus.
6.	Set first TAG address to Write.	
7.	Set CK input to logic 1.	AK output will go to logic 1. First address will echo to Output Bus.
8.	Set second TAG address to Write.	
9.	Set CK input to logic 0.	AK output will go to logic 0. Second address will echo to Output Bus.
10.	Repeat steps 6 to 9 until all addresses to be Written are loaded.	
11.	Set first Data for first address.	
12.	Set CK input to logic 1.	AK output will go to logic 1. First Data will echo to Output Bus.
13.	Set second Data for second address.	
14.	Set CK input to logic 0.	AK output will go to logic 0. Second Data will echo to Output Bus.
15.	Repeat steps 11 to 14 until all data to be Written are loaded.	
16.	Set CK and WR inputs to logic 0 to end programming.	AK output will go to logic 0. EC output will go to logic 1. Output Bus will clear to 0.

The Discontinuous Write command is now loaded into the CELB-81. The presence of a TAG in the Transceiver Transmission Zone is not necessary.

Stage 2 Writing to the TAG

1.	TAG enters into the Transceivers Transmissions Zone. PRE will go to logic 1.
2.	CELB-81 executes the programmed instruction and performs an absolute Data check.
3.	The EC output will go to logic 0.
4.	OC output will go to logic 1. This indicates the instruction has been successfully completed.
5.	When the TAG leaves the Transceivers Transmission Zone, PRE output will go to logic 0.

Stage 3 Verifying Command Execution

Action		Result
1.	Set RD input to logic 1.	
2.	Set CK input to logic 1.	AK output will go to logic 1. The Output Bus will echo the program code for the instruction just executed.
3.	Set CK input to logic 0.	AK output will go to logic 0. Output Bus will echo the number of bytes it wrote.
4.	Set CK input to logic 1.	AK output will go to logic 1. Output Bus will echo the Data Written to the first TAG address.
5.	Set CK input to logic 0.	AK output will go to logic 0. Output Bus will echo the Data Written to the second TAG address.
6.	Repeat 4 and 5 until all Data Written to the TAG has been verified.	
7.	Set CK and RD inputs to logic 0.	Output Bus will clear to 0.

Glossary

AK	Acknowledgment output echoes Clock input.
CK	Clock input. Used to strobe information into the CELB-81.
DEFB	Low TAG Battery output.
DF	General Fault output. Error in programming sequence or hardware (see Fault Table pg. 15 for specific fault).
E (TRANS)	Serial input terminal on Transceiver.
EC	Output line indicating CELB-81 is in the process of executing a command.
OC	Output line indicating operation is complete.
PRE	Output line indicating TAG is present in the Transceivers Transmission Zone.
RD	Input line. Enables retrieval of Data.
S (TRANS)	Serial output terminal on Transceiver.
WR	Input line used to enable programming of the CELB-81.

Fault Codes

Any Programming or Interrogation error will cause the DF output to switch HIGH. To obtain the fault code, Set RD = 1 and CK = 1, the fault code will appear on the Output Bus. The specific error can be analyzed from the table below.

*** These values are only valid if DF line is High.**

Fault Table

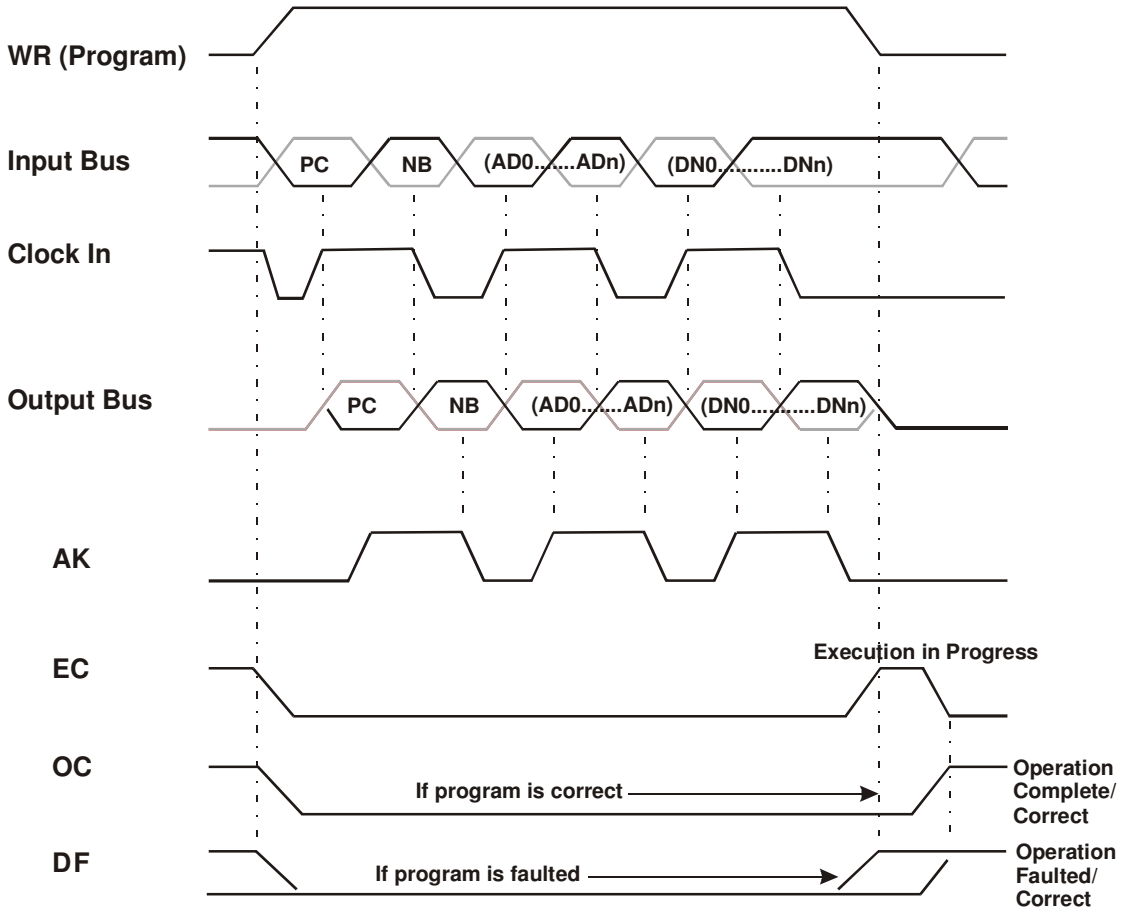
Fault Code	Fault Type	Cause
03H	Programming Error	Non-existent Instruction Buffer Full Incorrect number of bytes loaded Incorrect Memory Request Disallowed Address Data missing (Write)
0BH	Incorrect Memory request	Instruction for a 2K TAG given to a 64 byte TAG
0CH	Transceiver error	Transceiver wiring problem
0EH	TAG fault	Failed TAG or Corrupt Memory; Re-initialize the TAG
0FH	TAG to Transceiver fault	Dialog interrupted The TAG is absent Interference with the Transceiver

CELB-81 Wiring

Terminal	Symbol	Function
1	E (Trans)	
2		
3	DEFB	Status Outputs
4	PRE	
5	DF	
6	OC	
7	EC	
8	AK	
9	O-0	Output Bus
10	O-1	
11	O-2	
12	O-3	
13	O-4	
14	O-5	
15	O-6	
16	O-7	

Terminal	Symbol	Function
17	WR	Command Inputs
18	RD	
19	CK	
20	I-7	Input Bus
21	I-6	
22	I-5	
23	I-4	
24	I-3	
25	I-2	
26	I-1	
27	I-0	
28		
29	S (Trans)	
30	+24 V DC	Power Supply
31	Ground	

Programming Timing Chart



PC = Programming Code
NB = Number of bytes

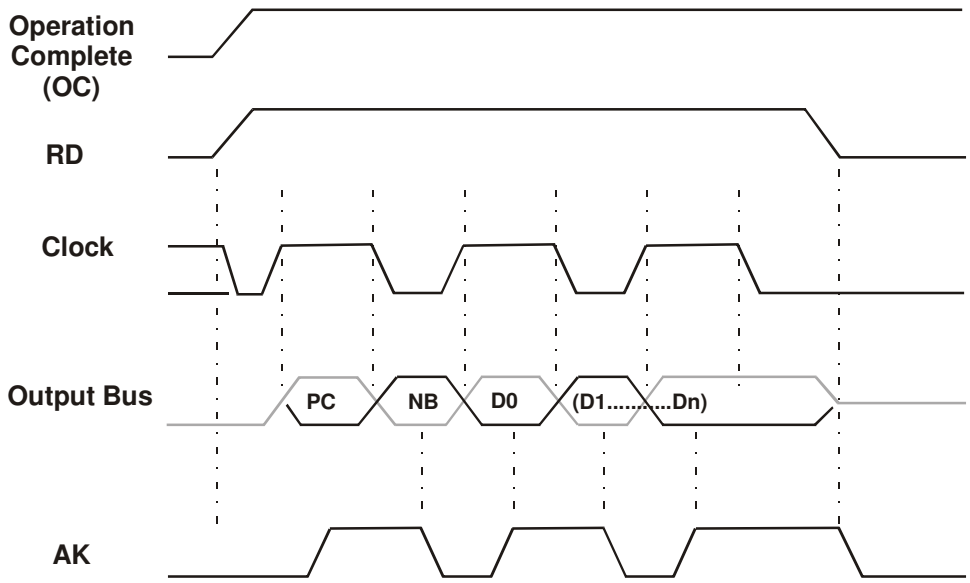
ADn = Address
DNn = Data value

TAG Block Read/Write time = 50ms + (10ms x n)
n = Number of bytes

TAG Discontinuous Read/Write time = 40ms + (20ms x n)
n = Number of bytes

NOTE: To cancel a programming operation raise Input Lines WR & RD to logic 1 (HIGH) simultaneously (Hold HIGH for 100ms).

Retrieval of Data after Operation Complete

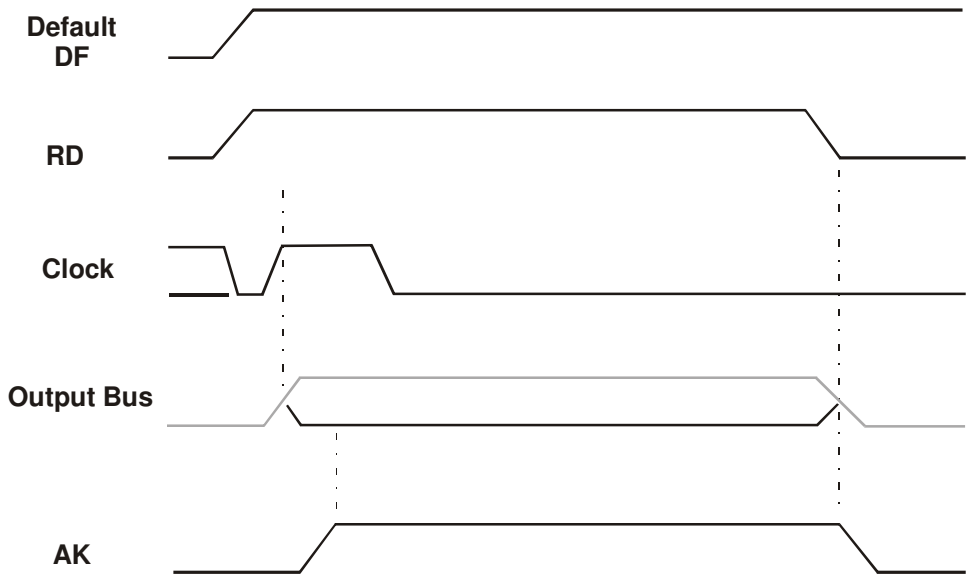


PC = Programming Code

NB = Number of bytes

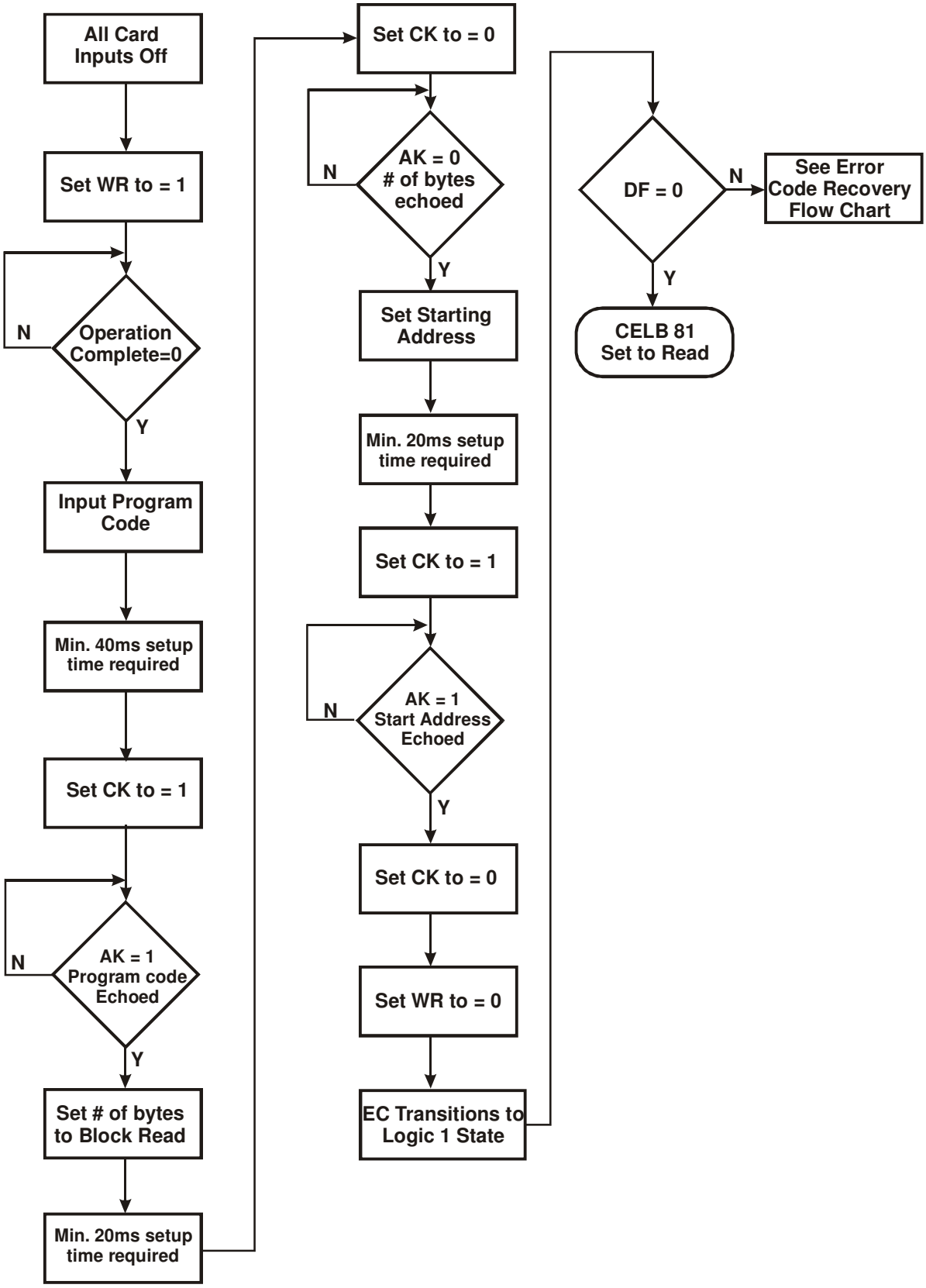
Dn = Data Value

Retrieval of Fault Data after Operation Complete

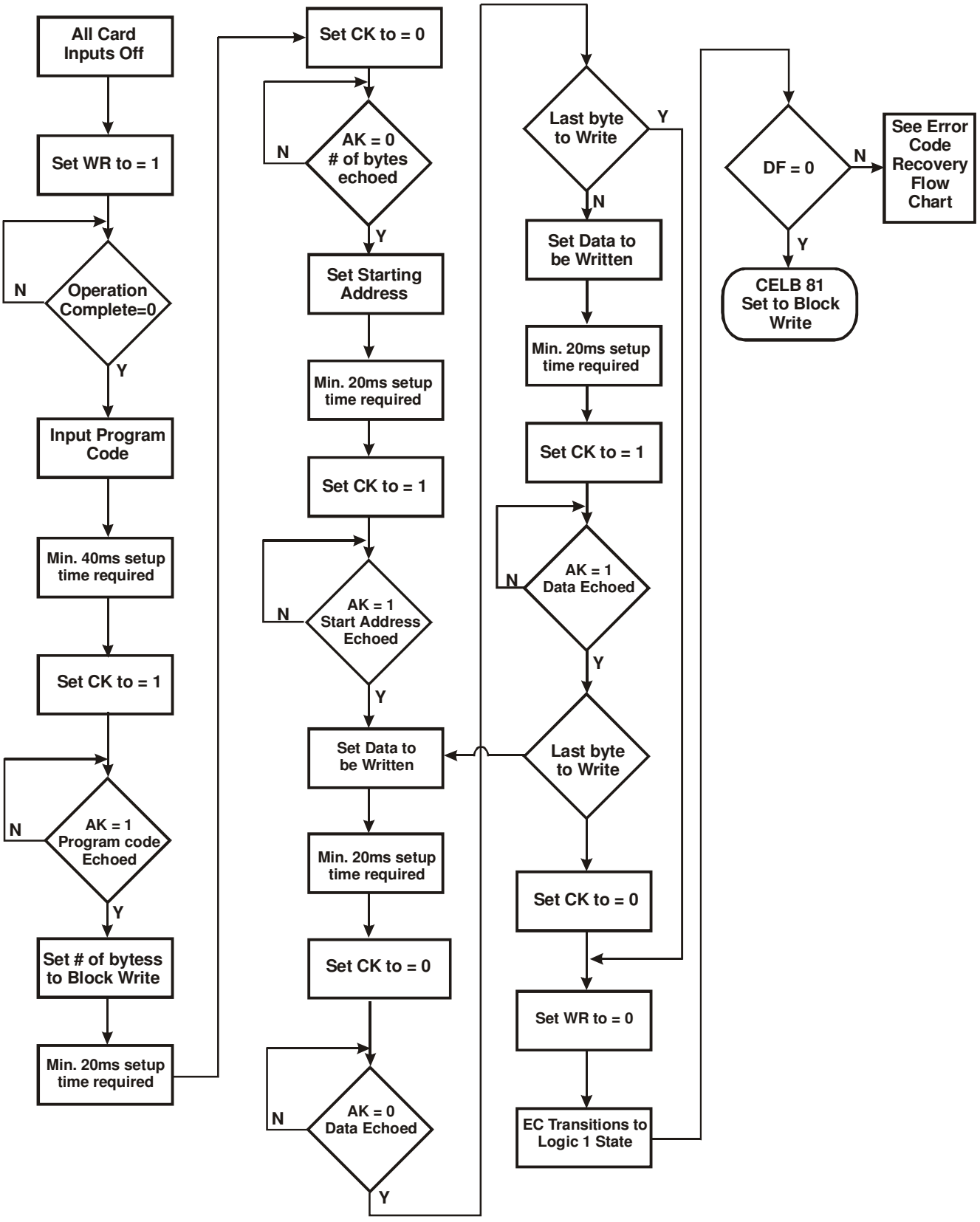


NOTE:
See Fault Code Chart on Page 15 for Explanation of fault types and causes.

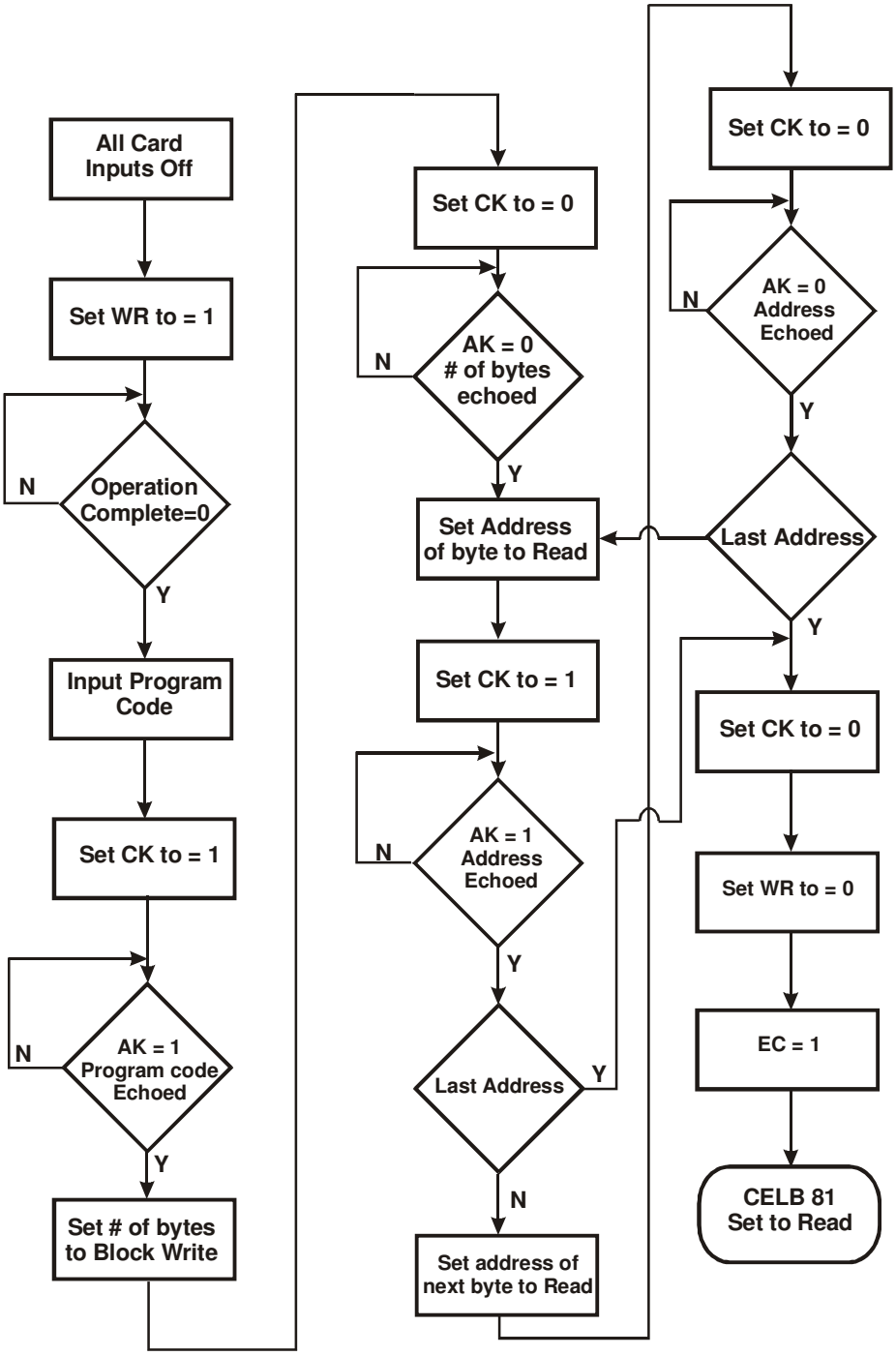
Programming Flow Chart for Block Read



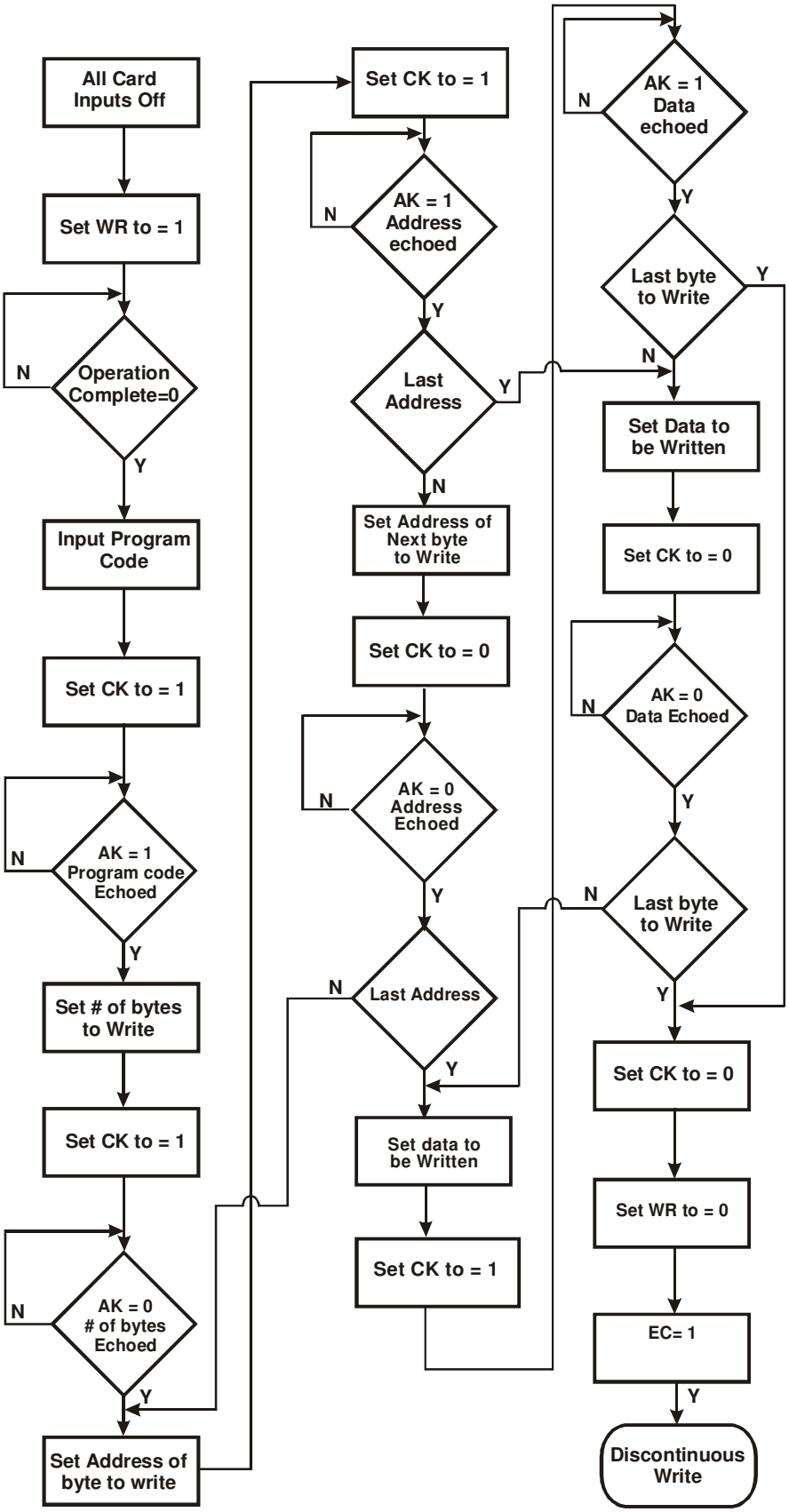
Programming Flow Chart for Block Write



Flow Chart for Discontinuous Read

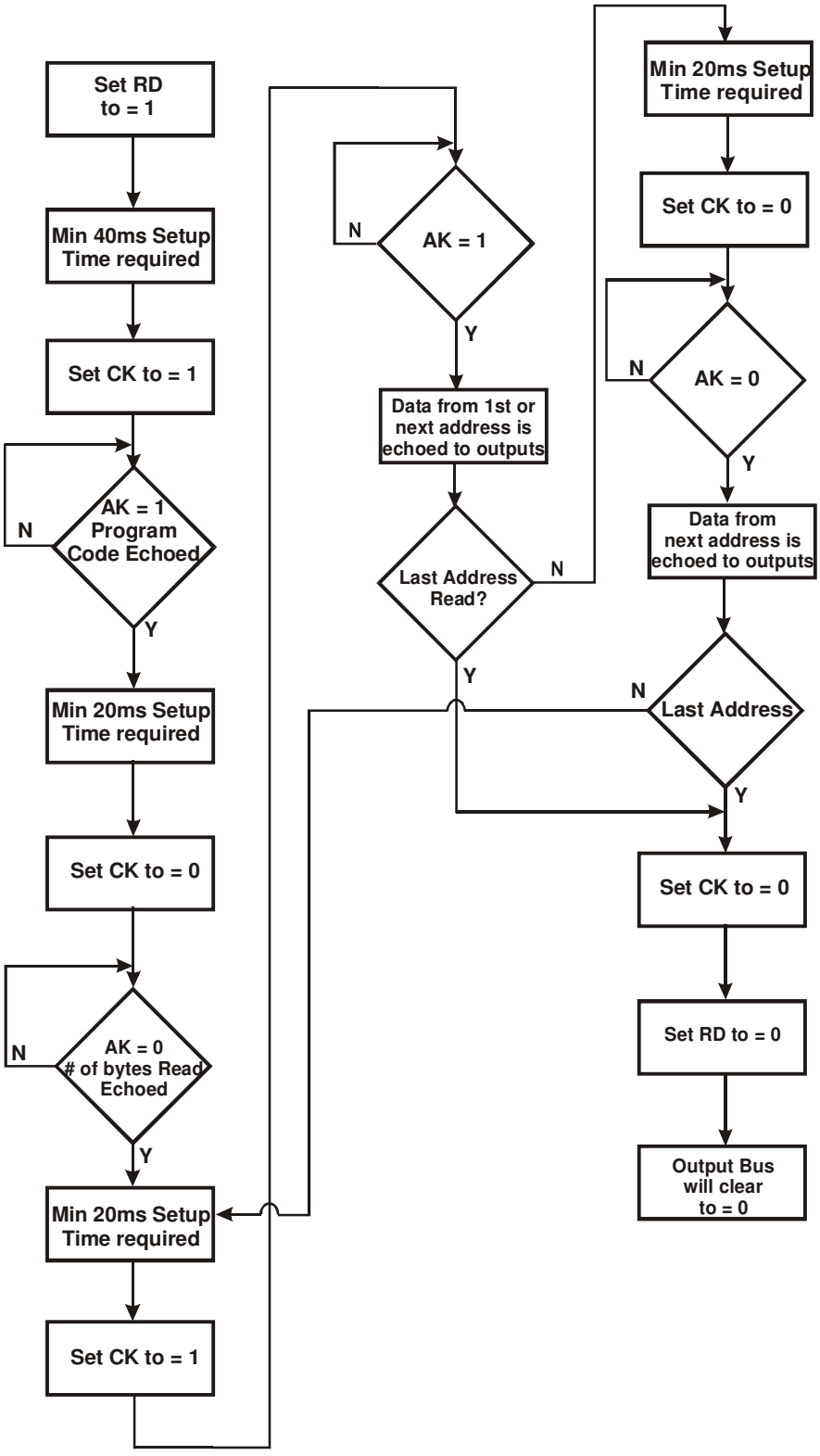


Flow Chart for Discontinuous Writes

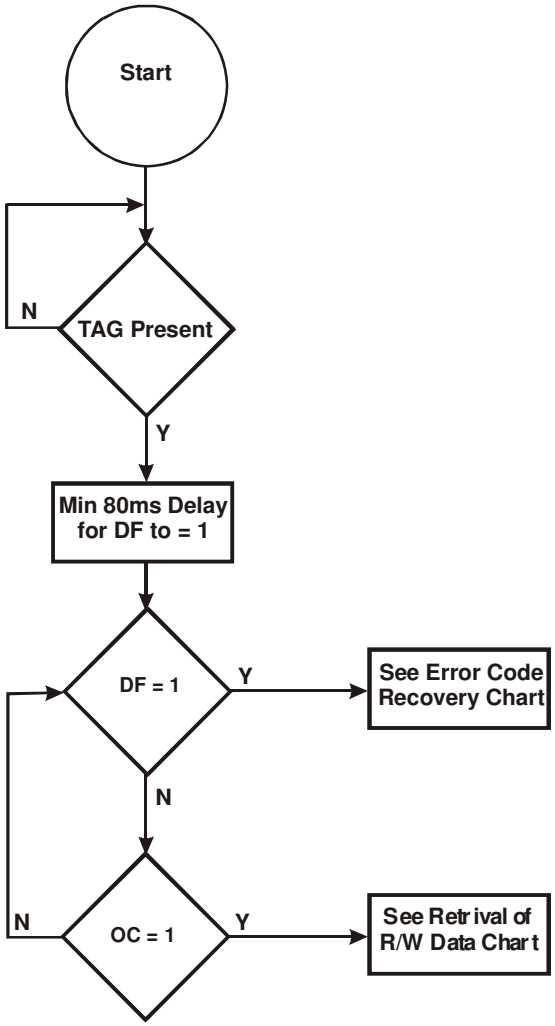


Retrieval of Read/Write Data Flow Chart

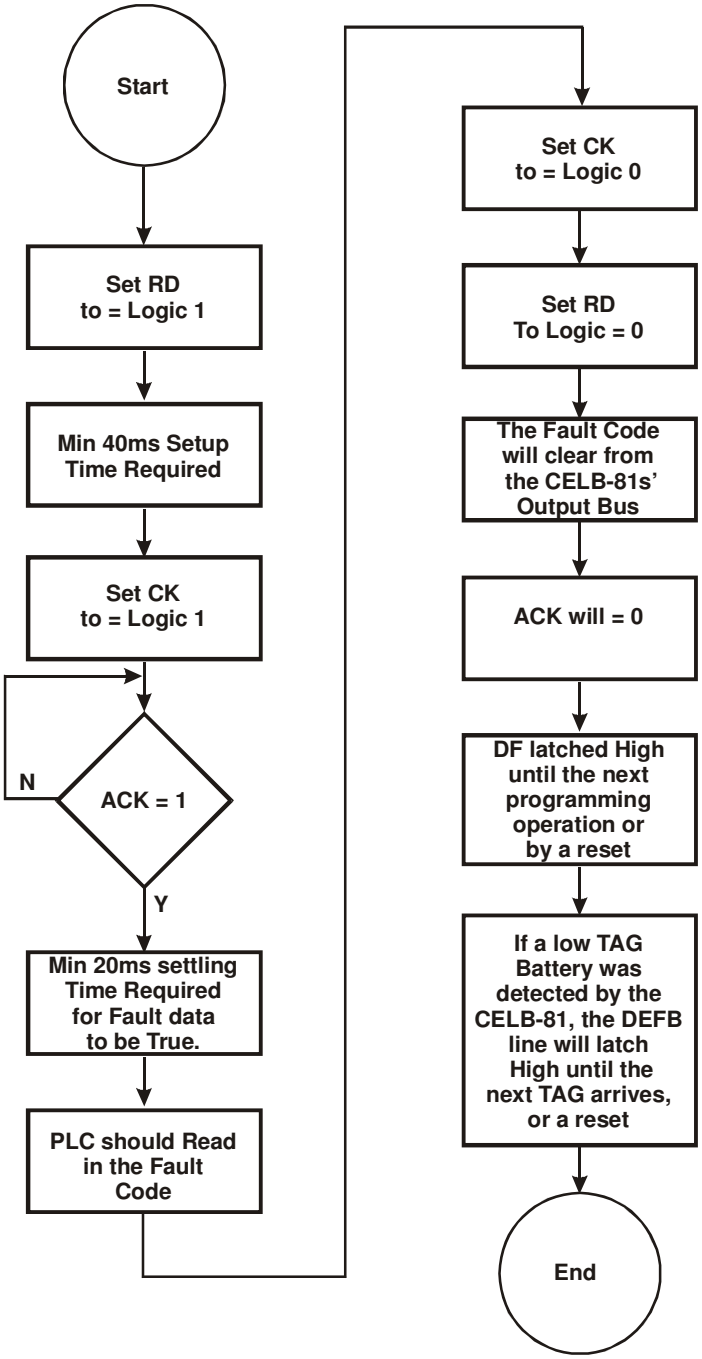
Block Mode



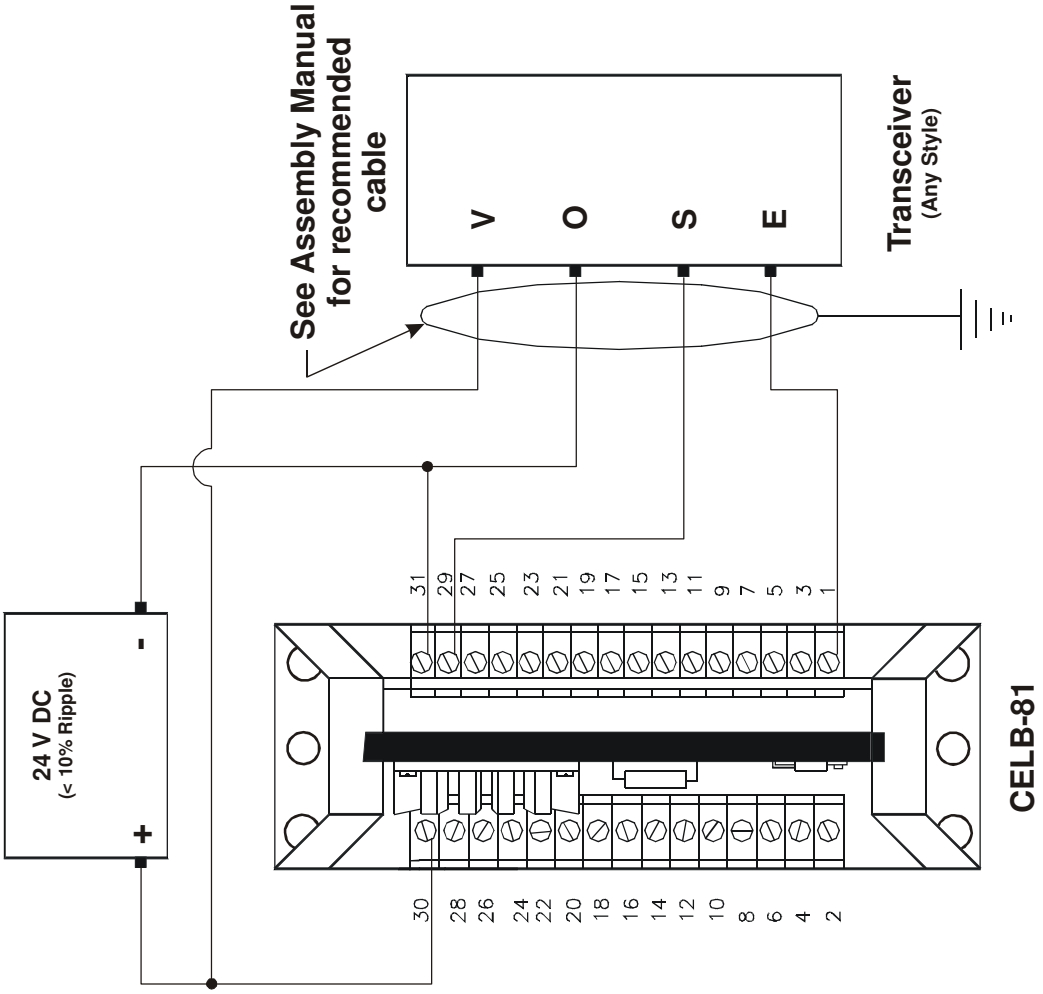
Read/Write Operation in Progress Chart



Error Code Recovery Flow Chart



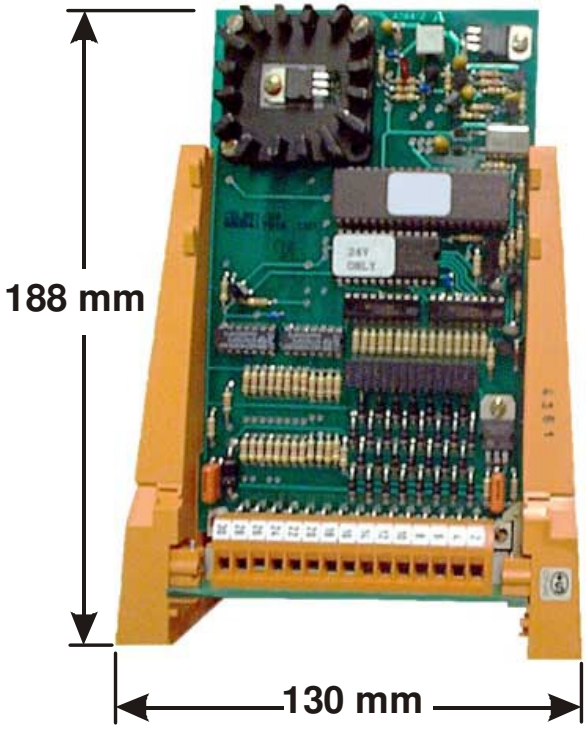
Connections



PLC Connections (Parallel I/O)	Input/Output From PLC	CELB 81 Terminals
PLC Output Address and Data	↑	20 MSB
	↑	21
	↑	22
	↑	23
	↑	24
	↑	25
	↑	26
	↑	27 LSB
PLC Input Address and Data	↓	9 LSB
	↓	10
	↓	11
	↓	12
	↓	13
	↓	14
	↓	15
	↓	16 MSB
Battery Fault	↓	3 DEFB
TAG Present	↓	4 PRE
General Fault	↓	5 DF
Operation Complete	↓	6 OC
In Process	↓	7 EC
Acknowledgment	↓	8 AK
Programmer Enabler	↑	17 WR
Retrieve	↑	18 RD
Clock	↑	19 CK

Note: The Transceiver can be located up to 300 M from the Control Board

CELB – 81 Control Board



- Electronic Control Card. Eurocard Format (100 x 160mm).
- Allows Reading and Writing of type “OMA” 64 byte or 2K byte TAGS.
- Reads or Writes blocks of data (77 bytes Continuous Format, 38 bytes Discontinuous Format).
- Each Control Board must be connected to a BALOGH Transceiver in order to Read/Write data from the TAGS.

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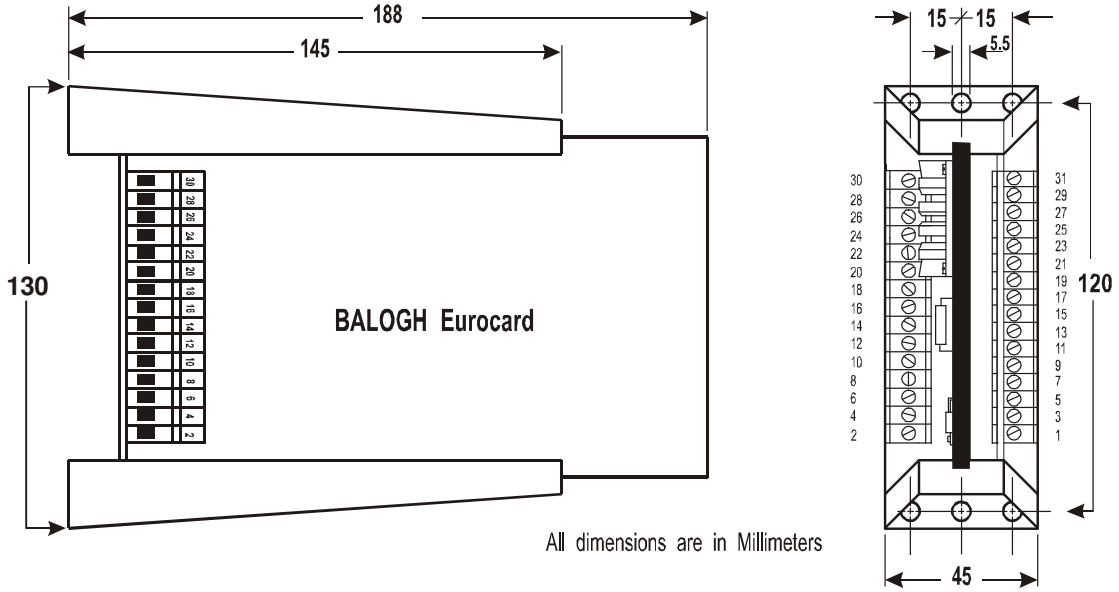
Characteristics at 25° C	Symbol	Unit	CELB-81
V Supply (< 2% Ripple)	Vcc	V DC	24
Voltage Tolerance			-10% to +10%
Current Consumption	Im	mA	150
Serial Connection			No
No. of Parallel Inputs			11
Input Impedance	Ze	K ohm	10
Input Logic 0		V	0 to 10
Input Logic 1		V	15 to Vcc
No. of Parallel Outputs			14
MAX Continuous Current (per Output)	Is	mA	100
MAX Voltage Drop across an Output	Vdrop	V	1.5
Output Logic 0		V	0
Output Logic 1		V	Vcc – 1.5
MIN Ambient TEMP	Tmin	℃	0
MAX Ambient TEMP	Tmax	℃	+70
Protection Degree	IP		00
Weight	M	g	300
MAX Cable Length Between Control Board and Transceiver			1000 ft
Short Circuit Protected			Yes
Protected against Inverse Polarity			Yes

CELB – 81 Control Board



Terminal	CELB-81 Locations	ER *71/85	ER *80
1	Transceiver Output Connected to	E	Term 3
2			
3	DEFB OUTPUT		
4	PRE OUTPUT		
5	DF OUTPUT		
6	OC OUTPUT		
7	EC OUTPUT		
8	AK OUTPUT		
9	Bit 0 OUTPUT (LSB)		
10	Bit 1 OUTPUT		
11	Bit 2 OUTPUT		
12	Bit 3 OUTPUT		
13	Bit 4 OUTPUT		
14	Bit 5 OUTPUT		
15	Bit 6 OUTPUT		
16	Bit 7 OUTPUT (MSB)		
17	WR INPUT		
18	RD INPUT		
19	CK INPUT		
20	Bit 7 INPUT (MSB)		
21	Bit 6 INPUT		
22	Bit 5 INPUT		
23	Bit 4 INPUT		
24	Bit 3 INPUT		
25	Bit 2 INPUT		
26	Bit 1 INPUT		
27	Bit 0 INPUT (LSB)		
28			
29	Transceiver Input Connected to	S	Term 2
30	+24 V DC to Board & Transceiver	V	Term 1
31	Ground	O	Term 4

* Locations on Transceivers

The letters indicating “EOSV” are located inside the Transceiver’s connection chamber or on the chamber’s top.

Note: When using BALOGH Transceivers Cables E is Blue, S is White, V is Brown, O is Black